REMARKS

In accordance with the foregoing, claims 1-8 are amended to address formalities and new claims 9-10 are added. No new matter is presented in any of the foregoing and, accordingly, approval and entry of the amended claims are respectfully requested.

Claims 1-10 are pending. Reconsideration is requested.

Traverse Of Rejection

Applicants note that page 3, lines 6-7 of the Office Action indicate that claims 1-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Abe (Pub. No. US 2003/0136577).

While page 3, lines 8-19 of the Office Action indicate that claims 1-8 are also rejected under 35 U.S.C. §102(e) as being anticipated by Abe, the Examiner supports the rejection on pages 3-5 of the Office Action only with an attempt to establish *prima facie* obviousness.

As discussed in the telephone call between the Examiner and the Applicants' representative, the Examiner indicated the statements on page 3, lines 8-19 as the rejection of claims 1-8 being under 35 U.S.C. §102(e) are in error and to be disregarded, and instead claims 1-8 are rejected only under 35 U.S.C. §103(a).

Accordingly, this response traverses the rejection of claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Abe.

Independent claim 1 recites a semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, "wherein: the core substrate being of a material having a heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate. (emphasis added)."

That is, according to independent claims 1 and 5, the specific characteristics of strength and/or elongation of the outermost resin layer are different from the specific characteristics of strength and/or elongation of the inner resin layer.

As set forth in MPEP §2143.03 "To establish *prima facie* obviousness of a claimed

invention, all the claim limitations must be taught or suggested by the prior art."

Abe does not teach that the specific characteristics of strength and/or elongation are different respectively for an outermost resin layer and inner resin layer. The Action concedes that Abe does not teach:

> material for the core substrate is selected so that it is closer to that of a semiconductor chip than the respective heat expansion coefficients of the main resin layers 14, 22, 26, 30 (fig. 1) and the interconnect patterns 20, 24, 28 (fig. 1).

(Action at page 4).

However, the Examiner asserts it would have been obvious:

> to construct the invention of Abe with the selection of materials as provided in Table 1, since it is (a) prima facie obvious to an artisan for optimization and experimentation to select the available materials in Table 1 for the advantage of preventing cracking, deformation, and other problems arising in the substrate due to the thermal stress occurring between the core substrate and the inner resin layers in the substrate and interconnect patterns in the substrate . . . the resin layers 14, 22, 26, 30 (fig. 1) can be selected among the disclosed group of materials . . . so as to provide the outermost layer with the higher strength and elongation than the inner layer.

(emphasis added, action at page 4).

Applicants submit the Examiner's assertions do not establish *prima facie* obviousness. As set forth in MPEP §2143.01 entitled Suggestion or Motivation To Modify the References:

> Obviousness can only be established by . . . modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

Applicants submit that Abe does not suggest a motivation for a modification to solve a problem of stress as the Examiner asserts. In particular, Abe does not suggest to one of ordinary skill in the art experimentation so as to configure a device substrate such that both:

(1) a core substrate "of a material having a heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns," and

(2) a resin layer, "forming an outermost layer . . . of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate."

By contrast, Abe teaches:

> (i)n the case that the multi-level interconnection layers are formed on both surfaces of the core substrate, stress due to the thermal expansion coefficient difference are substantially offset between the front side and the back side. On the other hand, in the case that the multi-level interconnection layer is formed only on one surface of the core substrate, the stress is exerted as they are to the core substrate, but the core substrate of the present embodiment having high rigidity can exert desirable characteristics even in applications when the multi-level interconnection layer is formed only on one surface of the core substrate.

(paragraph [00703], emphasis added).

That is, Abe teaches, regardless of the embodiments discussed therein, any problems that would have occurred due to stress are "offset."

Applicants submit the Examiner is incorrect in her assertion that it would have been obvious for "an artisan for optimization and experimentation to select the available materials in Table 1" to prevent stress.

In addition, Abe teaches that:

> (t)he resin material forming the insulating layer 14 is suitably polyimide resin, but polyimide resin is not essential. The resin material can be a resin having good heat resistance and insulation, such as polyetherimide, polyethersulfone, epoxy resin, tetrafluoroethylene, polyurethane resin, silicone resin, acrylic resin, bismaleimide-triazine (BT) resin or others.

(paragraph [0063], emphasis added).

Since Abe discusses material selection based merely on heat resistant properties, Applicants submit that one of ordinary skill in the art would not have further investigated materials for specific strength and elongation relationships, as recited by claims 1-8.

Summary

Since *prima facie* obviousness is not established, the rejection should be withdrawn and claims 1-8 allowed.

New Claims 9-10

New claims 9-10 are presented to recite features in a different fashion. Claim 9 recites a substrate for a chip, comprising: "a first resin layer forming an outermost layer on each of opposite main surfaces of the substrate; a second resin layer underlying the first resin layer; a third resin layer underlying the second resin layer; and a core underlying the third resin layer having, on both main surfaces, respective interconnect patterns . . . , wherein at least one of the first resin layer and the second resin layer being of a material having at least one of a higher strength and a higher elongation than a material used for the third resin layer."

Claim 10 is dependent on claim 9. Support for claims 9-10 is found, for example, in page

11, paragraph [0024].

These, and other, features of claims 9-10 patentably distinguish from the cited art, and they are submitted to be allowable for the recitations therein.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. And further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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